ABSTRACT OF THE DISCLOSURE

A multiprocessor system in which an interrupt generation unit of a first processor generates an interrupt to a second processor when a predetermined call instruction is executed in a running main routine. An address save unit of the second processor saves a return address for returning to the main routine upon completion of processing of a subroutine called by the call instruction to a predetermined memory area when it receives the interrupt from the interrupt generation unit. The interrupt generation unit generates an interrupt to the second processor again when a predetermined return instruction is executed in the subroutine. An address notification unit of the second processor notifies the return address to the first processor when it receives the re-generated interrupt. Processing is thus flexibly executed with the circuits of small sizes.